CLAIMS

Having thus described my invention, what I claim as new and desire to secure by Letters Patent is as follows:

1. A method of adjusting carrier mobility in semiconductor devices comprising the steps of

depositing a first stressed film on a wafer including first and second transistors to create a stress in the channels of the transistors,

partially removing said first stressed film to relieve said stress from a channel of one said transistor,

depositing a second stressed film over first and second transistors to apply a second stress to the channel of the transistor having said first stressed film removed.

2. A method as recited in claim 1 in which first transistor and second transistor are of different conductivity types.

3. A method as recited in claim 2 in which first film and second film apply opposing stresses.

4. A method as recited in claim 3 wherein the carrier mobility is regulated by applying tensile stress to said first transistor while applying compressive stress to said second transistor.

5. A method as recited in claim 4 wherein at least one stressed film is applied using plasma enhanced chemical vapor deposition (PECVD).

6. A method as recited in claim 4 wherein at least one stressed film is applied using thermal chemical vapor deposition (CVD).

7. A method as recited in claim 5 wherein at least one stressed film is applied using thermal(CVD).

8. A method as recited in claim 4 further comprising the steps of:

partially or fully removing first stressed film from both first and second transistors as masked by an oxide layer;

removing said oxide layer and depositing a shear force isolation layer across entire CMOS pair;

applying a blocking layer to first transistor and associated portions of said layers/films;

removing layer/film portions associated with said second transistor;

removing said blocking layer from said first transistor; and

depositing said second stressed film over the first and second transistors.

9. A method as recited in claim 4 further comprising the steps of:

applying a blocking layer to said first transistor;

partially or fully removing said first stressed film from second transistor;

removing said blocking layer from said first transistor; and

applying said second stressed film over the first and second transistors.

10. A structure that adjusts carrier mobility in CMOS transistors comprising:

a substrate,

a first transistor having a gate dielectric, gate electrode, and source, drain, and gate silicide regions, formed on said substrate,

a second transistor having a gate dielectric, gate electrode, and source, drain, and gate silicide regions, formed on said substrate,

a first film providing tensile stress at least at the channel of first transistor,

a second film providing compressive stress at least at the channel of second transistor, and

a shear force isolation layer separating said first film and said second film in at least one area.

11. A structure as recited in claim 10 wherein the first and second films can be composed of nitride, oxide, or other material that exhibits either tensile or compressive properties.

12. A structure as recited in claim 11 wherein the first and second stressed films are separated by a shear force isolation layer at all points.

13. A structure as recited in claim 12 wherein the first stressed film, closer to the substrate than the second stressed film, does not fully surround the nMOS transistor, but rather the sides only, while the remaining surfaces of the nMOS transistor are contacted by said shear force isolation layer.

14. A structure as recited in claim 13 wherein said shear force isolation layer is the only separation between the nMOS transistor and said second film.

15. A structure as recited in claim 13 wherein said shear force isolation layer surrounds the majority of the oxide liner of the pMOS transistor gate electrode except the top of the gate which engages directly with said second stressed film.

16. A structure as recited in claim 11 wherein the first and second stressed films are separated by a shear force isolation layer at selected areas.

17. A structure as recited in claim 16 wherein the first stressed film, closer to the substrate than the second stressed film, fully surrounds the nMOS transistor.

18. A structure as recited in claim 17 wherein said first stressed film is the only separation between the nMOS transistor and said second stressed film.

19. A structure as recited in claim 17 wherein said second stressed film surrounds the oxide liner at the sides of the pMOS transistor gate electrode with the top of the gate directly engaged with said second stressed film.